

GaAs MONOLITHIC TRANSFERRED-ELECTRON DEVICES FOR MILLIMETER WAVE APPLICATIONS

P.A. ROLLAND, A. CAPPY, M.R. FRISCOURT

Centre Hyperfréquences et Semiconducteurs
 Laboratoire Associé au C.N.R.S. n° 287
 Université de Lille I - 59655 VILLENEUVE D'ASCQ CEDEX - FRANCE

ABSTRACT

In this paper the authors point out the existence of two different operating modes in a planar GaAs transferred-electron oscillator with a current limiting MESFET cathode. The respective advantages and drawbacks of these two modes are discussed on the basis of further monolithic integration. The influence of the operating conditions on the RF performance are given in the 100 GHz window.

INTRODUCTION

In previous works we have studied the behaviour of long InP mesa devices, with a Schottky contact as a current limiting cathode contact in the 100 GHz window [1]. We have shown that these devices can be operated in an efficient overlength "dipolar-layers" mode inducing a more or less uniform electric field distribution throughout the entire active zone of the device. This feature allows the device to be operated under high RF voltage swing conditions, and consequently yields very interesting RF performance. For instance, output power up to 280 mW and 10 % conversion efficiency were predicted in the vicinity of 100 GHz with overcritically doped structures. Besides, this operating mode is rather insensitive to transit effects, and thus this kind of current limiting cathode contact devices can be operated from the transit frequency corresponding to the device length, up to the intrinsic cut-off frequency of the negative differential mobility. The limitation of the RF performance is then due to the minimal matchable impedance [2]. However the technology of such contact on InP is not yet reliable and in addition, in the case of GaAs devices, the typical Schottky barrier height is high, and the resulting reverse current is low. Thus this operating mode is not achievable with Schottky cathode contact GaAs mesa devices. Thus we have tried to obtain the same operating mechanisms by means of a planar diode with a MESFET controlled injection [3] [4].

THE MODEL

Figure 1 represents a schematic view of the studied device. To perform this study, we have used the analytical model we have previously developed, and already described elsewhere [5].

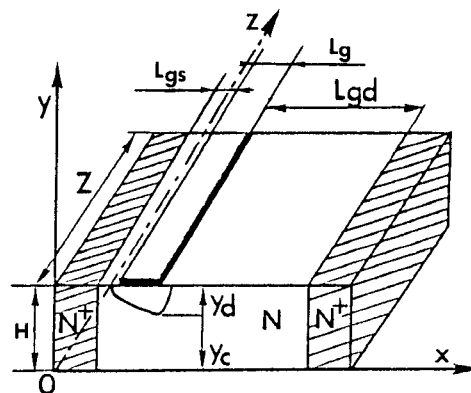


Figure 1 : Schematic view of the GaAs planar transferred-electron device.

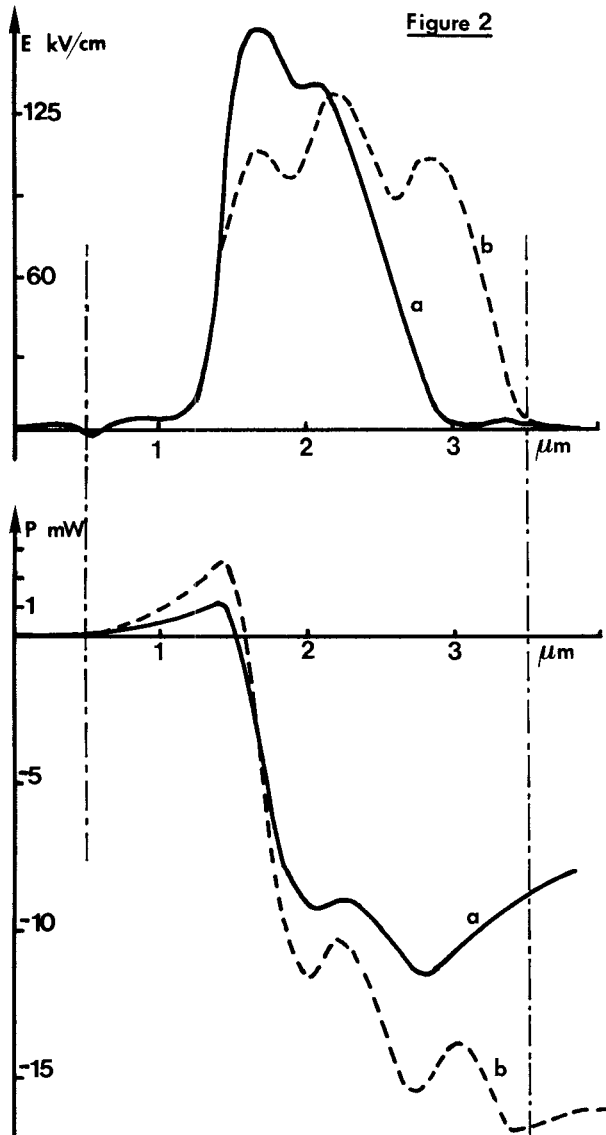
This unidimensional model takes into account spatial non-uniformity as well as non-stationary electron dynamics effects. It has been modified in order to account for some important two-dimensional effects (such as the depleted zone under the gate and the carrier injection into the buffer layer), following a simple method reported by A. CAPPY for FET's [6]. This one dimensional approach could be questionable especially near the drain edge of the gate, where bidimensional effects are predominant, but, it has been shown by A. CAPPY to be a quite good approximation for FET's behaviour. Within its limits this model allows us to describe all the physical phenomena involved from source to drain, without making any assumption on the current injection law and boundary conditions.

In the millimeter wave range our approach remains valid as long as we deal with oscillators applications. Indeed, one of the main assumption of our model is that there are no RF variations of the gate-source voltage since we solve only the one dimensional Poisson's equation.

THE OPERATING MODES

Two main operating modes were identified, depending on the relative values of the gate-source

and drain-source bias voltages. Figure 2 recalls the main operating mechanisms of each one. The first one could be named the "FET-mode". It resembles that described in reference [4]. The negative differential mobility effect is obtained at the end of the gate region. The active zone is confined to the high electric field region. In the other part of the device the electric field is lower than its threshold value. This zone corresponds to a positive resistance and yields RF power losses as illustrated in figure 3 where we have reported the evolution of the RF power along the device for the two operating modes.



Figures 2 and 3 : Spatial evolution of the electric field at an instant $t = T/4$ of a 100 GHz cycle (figure 2). Evolution of the emitted power along the device (figure 3).
 $T = 400^\circ\text{K}$; $F = 100\text{ GHz}$; $V_{DS} = 12\text{ V}$; $m = 40\%$
 $L_G = 0.5\text{ }\mu\text{m}$; $L_{GS} = 0.5\text{ }\mu\text{m}$; $L_{GD} = 2.0\text{ }\mu\text{m}$;
 $N = 210^{16}\text{ cm}^{-3}$; $H = 0.8\text{ }\mu\text{m}$; $Z = 250\text{ }\mu\text{m}$.
 a - FET mode - $V_{GS} = -5\text{ V}$
 b - dipolar layers mode - $V_{GS} = -2\text{ V}$.

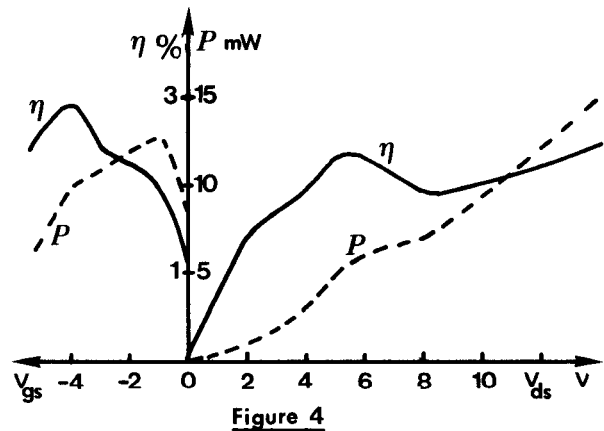
The second operating mode is quite similar to that we have reported for Schottky cathode contact InP mesa devices [1]. We can observe the propagation of dipolar layers, which yields a rather uniform spatial electric configuration (cf. figure 2). As for the previous operating mode the negative differential mobility effect is obtained at the end of the gate region. But here all the remaining N zone is active, as shown in figure 3.

INFLUENCE OF THE OPERATING CONDITIONS

Figures 4 and 5 illustrate the influence of the gate-source voltage and drain-source voltage on the available output power and terminal impedance. The transition between the two possible operating modes can be phenomenologically explained by the concept of the valley current $I = Aq N_D v_s$ [4]. The FET mode occurs for current injection level smaller than this valley current while dipolar layers mode occurs for injection level equal or slightly greater than this value. The injection level is controlled by the gate-source voltage V_{GS} . As shown in figure 4, there is a range of V_{GS} values for which the RF performance are nearly constant. This range corresponds to hydrid modes involving transit time effects in the depletion layer formed at the drain edge of the gate.

It can be noted that dipolar layers modes provide higher output power than true FET mode for the same terminal impedance level and also that these dipolar layers modes are nearly insensitive to the active (gate to drain) zone length which can range from 2 to 5 μm without power and impedance level degradation. This is an important feature for device realization and means that these devices can be operated from the transit frequency corresponding to the active device length up to the intrinsic cut-off frequency.

Figures 4 and 5 show that output power and terminal resistance increase with increasing drain to source voltage. Thus for such devices the limits will come from thermal limitation and from the intrinsic cut-off frequency of the negative differential mobility in GaAs ($\sim 120\text{ GHz}$).



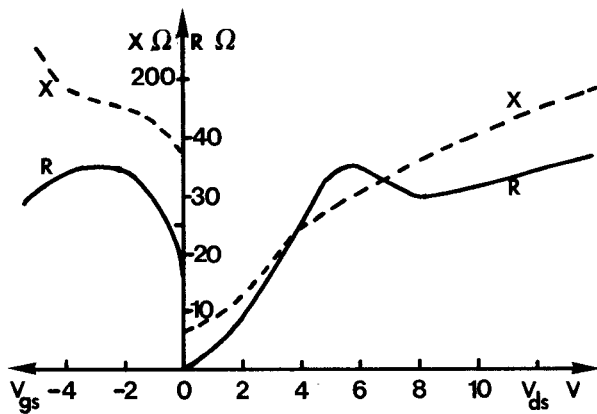


Figure 5

Figures 4 and 5 : Influence of the operating bias voltages (V_{gs} and V_{ds}) on the emitted power and conversion efficiency levels (Figure 4) and on the output impedance level (figure 5).
 $T = 400^\circ\text{K}$; $F = 100\text{ GHz}$; $m = 40\%$; $H = 0.8\text{ }\mu\text{m}$;
 $Z = 250\text{ }\mu\text{m}$; $L_G = 0.5\text{ }\mu\text{m}$; $L_{GS} = 0.5\text{ }\mu\text{m}$;
 $L_{GD} = 2.0\text{ }\mu\text{m}$; $N = 210^{16}\text{ cm}^{-3}$.

MONOLITHIC LOCAL OSCILLATOR APPLICATIONS

In order to realize discrete devices that are monolithic-compatible and GaAs-based several constraints must be satisfied.

The thermal resistance must not be too high in order to keep the operating temperature at an acceptable level ($T < 150^\circ\text{C}$) [7].

The gate width must be lower than $\lambda_g/10$ in order to avoid parasitic transversal propagation effects : $Z < 125\text{ }\mu\text{m}$ in our case at 100 GHz.

The terminal impedance level must be higher than the minimum matchable one with on-chip matching circuits. We have chosen a minimum terminal resistance of 10 Ω .

The Schottky contacts which are the more difficult technological operation on these devices can be replaced by a recess or a notch which simulate the depletion region created by the gate. The RF performance were found to be nearly unchanged. This was experimentally observed in the case of InP discrete devices [8]. We can emphasize that the gate length can range from 0.5 μm to 1.5 μm without significant variation of the RF performance.

On this basis a near optimum trade-off could be the arrangement shown in figure 6 which can provide with five elementary cells the following RF performance at 100 GHz :

$$P_{\text{out}} \sim 100\text{ mW} ; \eta = 3.6\% ; R = -10\text{ }\Omega ;$$

$$X = -104\text{ }\Omega ; 150^\circ < T < 200^\circ\text{C}$$

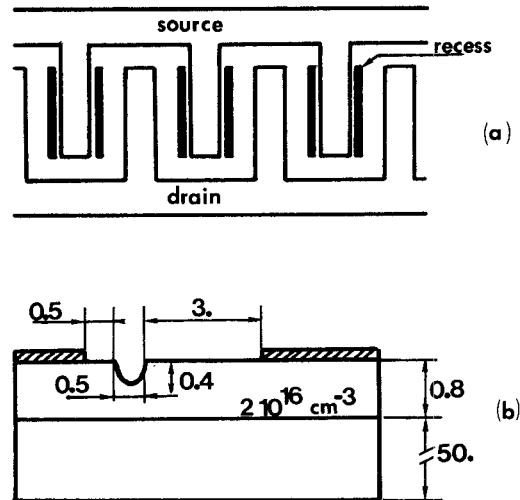


Figure 6 : Schematic view of a possible implementation of several elementary cells (a) and cross-sectional view of an elementary cell (b) (all dimensions are given in microns).

RF performance for each elementary cell $V_{DS} = 24\text{ V}$;
 $I_O = 23\text{ mA}$; $P = 20\text{ mW}$; $\eta = 3.6\%$; $R = -50\text{ }\Omega$;
 $X = -520\text{ }\Omega$;
 Over all performance for 5 cells $P = 100\text{ mW}$;
 $\eta = 3.6\%$; $R = -10\text{ }\Omega$; $X = -104\text{ }\Omega$; $T \sim 150^\circ\text{C}$.

Each elementary cell presents a gate width of 125 μm and a gate length ranging from 0.5 μm to 1.5 μm . The actual active zone length, namely the drain-gate length, is 3 μm . In fact, this later length is limited by thermal and impedance matching considerations. Indeed the RF performance are an increasing function of the drain-gate length, as can be seen in figure 7. But, obviously, the increasing drain-gate length results in a higher optimum drain-source bias voltage and hence a higher operating temperature. Besides, we must emphasize that the terminal reactance level also increases with the device length. This could involve some troubles for impedance matching the device. Thus the drain-gate length has been limited to 3 μm . The corresponding drain-source bias voltage is about 24 V. In the case of a three terminal device, the optimum gate-source voltage is -1 V. This also corresponds to a 0.40 to 0.45 μm recess depth for a 0.8 μm N layer, in the case of a two terminal device.

In addition, the modulation drive level ($m = V_{HF}/V_{DS}$) must not be too high, in order to keep the overall terminal resistance of the multi-cells device at a acceptable level. Indeed, as shown in figure 8, the output resistance level is a decreasing function of the modulation ratio. A modulation ratio value close to 60 % appears to be a good compromise since it allows to obtain interesting output power levels while keeping the elementary cell terminal resistance close to -50 Ω .

Finally, we can note that the semi-insulating substrate layer thickness must range between 50 and 75 μm , in order to minimize the thermal impedance.

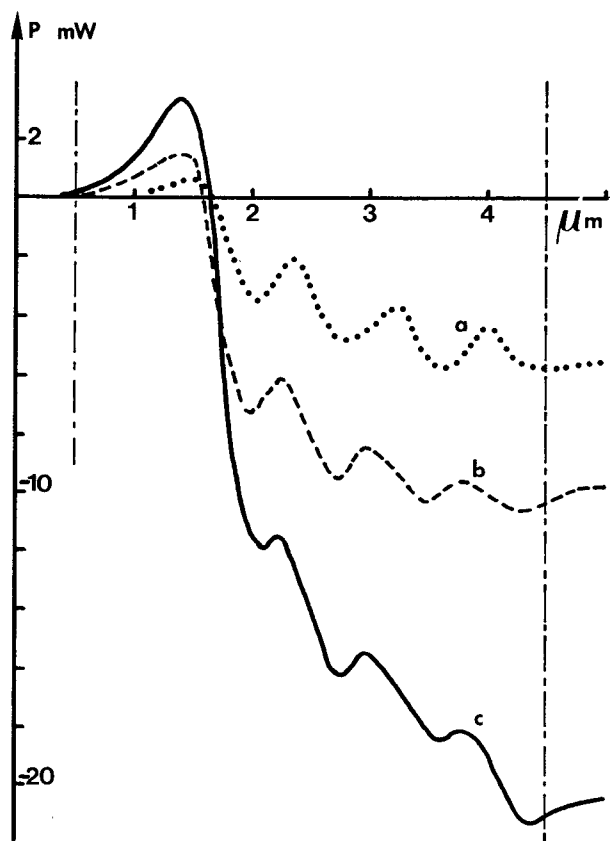


Figure 7 : Evolution of the emitted power along the device $F = 100$ GHz ; $V_{GS} = -1$ V ; $N = 210^{16}$ cm $^{-3}$; $L_G = 0.5$ μ m ; $L_{GS} = 0.5$ μ m ; $L_{GD} = 3.0$ μ m ; $H = 0.8$ μ m ; $Z = 125$ μ m.
a - $V_{DS} = 12$ V ; $m = 40$ %
b - $V_{DS} = 24$ V ; $m = 40$ %
c - $V_{DS} = 24$ V ; $m = 60$ %.

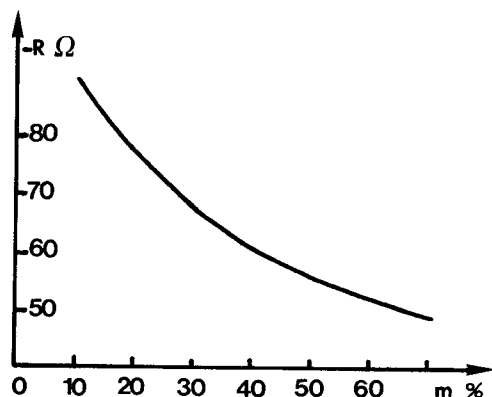


Figure 8 : Evolution of the elementary cell terminal resistance versus the modulation ratio ($m = V_{HF}/V_{DS}$). $T = 450$ °K ; $F = 100$ GHz ; $V_{DS} = 24$ V ; $V_{GS} = -1$ V ; $L_G = 0.5$ μ m ; $L_{GS} = 0.5$ μ m ; $L_{GD} = 3.0$ μ m ; $N = 210^{16}$ cm $^{-3}$; $H = 0.8$ μ m ; $Z = 125$ μ m.

CONCLUSION

Promising results were predicted in the 100 GHz window for planar GaAs Gunn devices. Either MESFET injection three terminal devices or recessed two terminal structures are monolithic-compatible which allow various circuit arrangements leading to function possibilities for the designer such as local oscillators and self oscillator mixers.

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